What is Claimed is:

[c1] 1. An I/O driver comprising:

a circuit adapted to be powered by a first power supply, said circuit adapted to receive a first signal referenced to the voltage of a second power supply and adapted to convert said first signal to a second signal of the same logical value as said first signal and referenced to the voltage of said first power supply, said circuit adapted to maintain said second signal on an output of said I/O driver when said second power supply is powered off.

[c2] 2. The I/O driver of claim 1, wherein the voltage of said first power supply is higher than the voltage of said second power supply.

[c3] 3. The I/O driver of claim 2, wherein the voltage of said first power supply is 2.5 volts or higher.

[c4] 4. The I/O driver of claim 1, wherein said circuit includes a level shifting circuit.

[c5] 5. The I/O driver of claim 4, wherein said level shifting circuit further includes a latching circuit.

[c6] 6. The I/O driver of claim 1, wherein said circuit includes a latching circuit.

[c7] 7. The I/O driver of claim 1, further including an output circuit coupled to an I/O pad of an integrated circuit chip.

[c8] 8. The I/O driver of claim 1, further including

a fencing circuit adapted to receive a fencing signal and a latching circuit adapted to latch said second signal in response to said fencing circuit receiving a fencing on signal.

[c9] 9. An I/O driver comprising:

a first circuit adapted to be powered by a first power supply, said first circuit adapted to receive a first signal referenced to the voltage of a second power supply and adapted to convert said first signal to a second signal of the same logical value as said first signal and referenced to the

voltage of said first power supply, said first circuit including a first latching circuit, said first latching circuit adapted to maintain the logical state of said second signal when said second power supply is powered off;

a second circuit adapted to be powered by said first power supply, said second circuit adapted to receive a third signal referenced to the voltage of said second power supply and adapted to convert said third signal to a fourth signal of the same logical value as said second signal and referenced to the voltage of said first power supply, said second circuit including a second latching circuit, said second latching circuit adapted to maintain the logical state of said fourth signal when said second power supply is powered off; and

a combinational logic circuit adapted to combine said second and fourth signals into a fifth signal and adapted to maintain said fifth signal on an output of said I/O driver when said second power supply is powered off.

[c10] 10. The I/O driver of claim 9, wherein the voltage of said first power supply is higher than the voltage of said second power supply.

[c11] 11. The I/O driver of claim 10, wherein the voltage of said first power supply is 2.5 volts or higher.

[c12] 12. The I/O driver of claim 9, wherein said first circuit includes a first level shifting circuit and said second circuit includes a second level shifting circuit.

[c13] 13. The I/O driver of claim 12, wherein said first level shifting circuit further includes a first latching circuit and said second level shifting circuit further includes a second latching circuit.

[c14] 14. The I/O driver of claim 9, wherein said first circuit includes a first latching circuit and said second circuit includes a second latching circuit.

[c15] 15. The I/O driver of claim 9, further including an output circuit coupled between said combinational logic circuit and said output of said I/O driver.

[c16] 16. The integrated circuit of claim 9, further including

a first fencing circuit adapted to receive a fencing signal and a first latching circuit adapted to latch said second signal in response to said first fencing circuit receiving a fencing on signal prior to powering down said first power supply; and

a second fencing circuit adapted to receive said fencing signal and a second latching circuit adapted to latch said fourth signal in response to said second fencing circuit receiving said fencing on signal.

[c17] 17. The I/O driver of claim 9, where in said combination logic circuit includes a NAND gate and a NOR gate.

[c18] 18. A method of maintaining the output state of an I/O driver when an integrated circuit chip is in a low power mode comprising:

providing a circuit adapted to be powered by a first power supply, said circuit adapted to receive a first signal referenced to the voltage of a second power supply and adapted to convert said first signal to a second signal of the same logical value as said first signal and referenced to the voltage of said first power supply, said circuit adapted to maintain said second signal on an output of said I/O driver when said second power supply is powered off.

[c19] 19. The method of claim 18, wherein the voltage of said first power supply is higher than the voltage of said second power supply.

[c20] 20. The method of claim 18, further including:

providing a fencing circuit adapted to receive a fencing signal; and

providing a latching circuit adapted to latch said second signal in response to said fencing circuit receiving a fencing on signal.